CLAIMS

What is claimed is:

1. A system for controlling an output voltage across a load using current mode control to control current through an output filter connected to the load, comprising:

an error amplifier for generating a reference current signal indicative of a desired average current through the load by comparing a voltage across the load to a reference voltage;

a differential current sensor having hysteresis that uses the reference current signal to generate a control signal indicating when an output current is greater than the desired average current; and

a current controller, responsive to the control signal to alternately couple the output filter to a first supply rail and to a second supply rail, to generate an average current through the load.

2. The system of claim 1, wherein the hysteresis of the differential current sensor is determined by an offset signal.

3. The system of claim 2, the current controller further comprising a positive power field-effect transistor (FET) and a negative power FET, the positive power FET coupling and de-coupling the output filter to and from the first supply rail, and the negative power FET coupling and decoupling the output filter to and from the second supply rail.

4. The system of claim 3, the differential current sensor further comprising a first positive reference FET that creates a voltage for comparison to the positive power FET, a second positive reference FET that creates a voltage for comparison to the negative power FET, the first and second positive reference FETs driven by the reference current when the desired output current is positive.

5. The system of claim 4, the differential current sensor further comprising a first negative reference FET that creates a voltage for comparison to the positive power FET, a second negative reference FET that creates a voltage for comparison to the negative power FET, the first and second negative reference FETs driven by the reference current when the desired output current is negative.

6. The system of claim 5, the positive power FET being constructed from X FETs that are substantially identical to the first positive reference FET and the first negative reference FET, such that the resistance of the positive power FET is 1/X of the first positive reference FET and the first negative reference FET, and the output current being X times the reference current.

7. The system of claim 6, wherein X is approximately 40,000.

8. The system of claim 5, the negative power FET being constructed from X FETs that are substantially identical to the second positive reference FET and the second negative reference FET, such that the resistance of the negative power FET is 1/X of the second positive reference FET and the second negative reference FET, and the output current being X times the reference current.

9. The system of claim 8, wherein X is approximately 40,000.

10. The system of claim 5, the differential current sensor further comprising a first comparator for comparing the voltage drop across the positive power FET with the voltage drop across the first positive reference FET plus the voltage drop across the first negative reference FET, the first comparator generating a first signal indicating that the output current is equal to or exceeds the desired average current plus an offset.

11. The system of claim 10, the differential current sensor further comprising a second comparator for comparing the voltage drop across the negative power FET and the second positive reference FET plus the second negative reference FET, the second comparator generating a second signal indicating that the output current is equal to or less than the desired average current minus an offset.

12. The system of claim 11, further comprising a driver that, in response to the first and second signals, alternately turns on (a) the positive power FET, the first positive reference FET, and the first negative reference FET, and (b) the negative power FET, the second positive reference FET, and the second negative reference FET.

13. The system of claim 2, wherein the offset signal is representative of half an allowable ripple on the output current.

14. The system of claim 13, wherein the offset signal is generated from a reference source within the system.

15. The system of claim 2, wherein the differential current sensor further comprises a differential current threshold detector for monitoring current in the load comprising:

a first transistor having a source, a drain, and a gate;

a second transistor having a gate coupled to the gate of the first transistor;

a third transistor having a gate coupled to the gate of the first transistor, a drain coupled to the load and to a source of the second transistor, and a source coupled to the source of the first transistor;

a first current source coupled to the drain of the first transistor;

a second current source coupled to the drain of the second transistor; and

a differential amplifier having a first input coupled to the drain of the first transistor and a second input coupled to the drain of the second transistor.

16. The system of claim 15, wherein a difference between a current of the first current source and a current of the second current source is a function of the offset signal.

17. The system of claim 15 wherein the third transistor serves as a switch of the current controller.

18. The system of claim 1, further comprising an external resistor connected between the load and the error amplifier, for determining the output voltage droop.

19. A differential current threshold detector for monitoring current in a load comprising:

a first transistor having a source, a drain, and a gate;

a second transistor having a gate coupled to the gate of the first transistor;

a third transistor having a gate coupled to the gate of the first transistor, a drain coupled to the load and to a source of the second transistor, and a source coupled to the source of the first transistor;

a first current source coupled to the drain of the first transistor;

a second current source coupled to the drain of the second transistor; and

a differential amplifier having a first input coupled to the drain of the first transistor and a second input coupled to the drain of the second transistor.

20. The differential current threshold detector of claim 19 having an output coupled to an output of the differential amplifier and wherein the differential current threshold detector has a threshold determined by a difference between a current of the first current source and a current of the second current source, and device sizes of the first, second, and third transistors.

21. The differential current threshold detector of claim 20, wherein the first and the second current sources are current mirrors.

22. The differential current threshold detector of claim 19, further comprising a threshold determined by a device size ratio of the first current source to the second current source.

23. A method for controlling an output voltage across a load, comprising:

comparing the output voltage across the load to a reference voltage;

generating a reference current signal indicative of a desired average current through the load;

generating a control signal indicating when an output current is greater than the desired average current; and

alternately coupling an output filter to a first supply rail and to a second supply rail in response to the control signal, to generate an average current through the load.

24. The method of claim 23, the control signal having hysteresis;

25. The method of claim 24, the hysteresis being determined by an offset signal.

26. The method of claim 23, the step of comparing comprising determining a voltage droop via an external resistor connected to the load.